PRELIMINARY DATA SHEET

CF2140

4 x SPST DC-6 GHz Switch Array

Features

- Normally open configuration
- True DC operation with Low 3 Ω Ron
- **DC current capability 250mA per SPST**
- **Pulse current 1A @ 125µs pulse width per SPST**
- Low capacitance for operation to 6 GHz
- High stand-off voltage of 120 V
- Less than 1 nA leakage current
- Fast switching time of 10 µs
- Low power consumption from 3.3 VDD
- Small 4 x 6 mm footprint for 3x higher density than competing solutions
- Serial or parallel control with daisy-chaining capability
- Endurance rated to 20M switching cycles

Applications

- AC/DC Switching
- Test & Measurement
- Matrix switching
- TRX filter tuning
- Impedance tuning
- High-power RF switching
- MRI / Ultrasound signal switching

Product Description

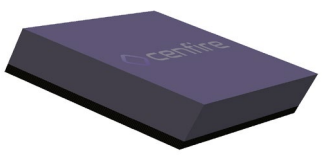
The CF2140 4xSPST switch array is based on the CenFire™ low-loss switching technology platform. This highly versatile product supports a wide variety of applications in signal switching and tuning with an emphasis on large-scale matrix switching and high current applications.

The CF2140 integrates four low-loss, fully symmetric high-voltage SPST switches with a flexible serial or parallel control interface. These switches offer industry leading capability combining wide bandwidth with DC offset voltage support, small area and low height, and zero leakage current, making them ideal for multiplexing source and measurement units as well as routing high-speed digital signals. Additionally, the high 120 V tolerance enables new applications such as RF filter tuning. The switches are normally open when off or even unpowered and cannot self-actuate.

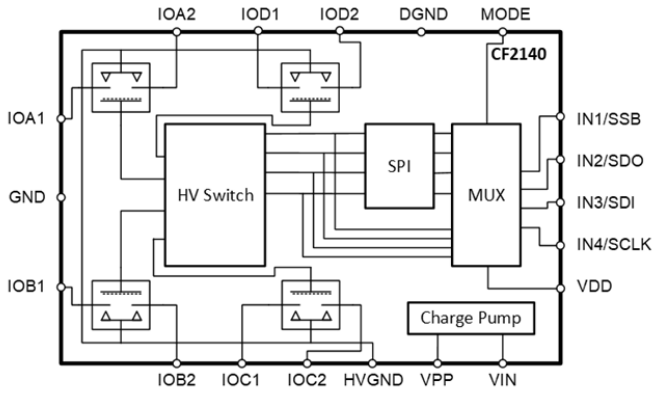
The unique, patented CenFire™ approach represents a breakthrough in MEMS switch technology, providing greatly enhanced performance, capability, and reliability versus traditional solutions such as electromechanical relays, reed relays, and optocouplers.

Package Diagram

36-lead 4 x 6mm LGA package



FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

25°C, V_{DD} = 3.3 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
On Resistance	R_{ON}	Resistance between SPST terminals 1 and 2		3		Ω
On Capacitance	C_{GND}	Parasitic capacitance to ground in On state		0.2		pF
Insertion Loss	IL	100 MHz 1000 MHz 3000 MHz 6000 MHz		0.15 0.3 0.4 0.6		dB
Isolation	ISO	100 MHz 1000 MHz 3000 MHz 6000 MHz		70 50 40 30		dB
Leakage Current	I_{LK}	Leakage current from SPST terminals 1 or 2 to any other pin			1	nA
Switching Time	t_{SW}	State change to within specification for IL or Isolation		10		µs
Start-up Time	t_{START}	Time from VDD within specification to all performances within specification		10		ms
Switching Period	t_{CHARGE}	Minimum time between switching events	100			µs
SPI Clock Frequency	f_{CLK}				10	MHz

OPERATING RANGES

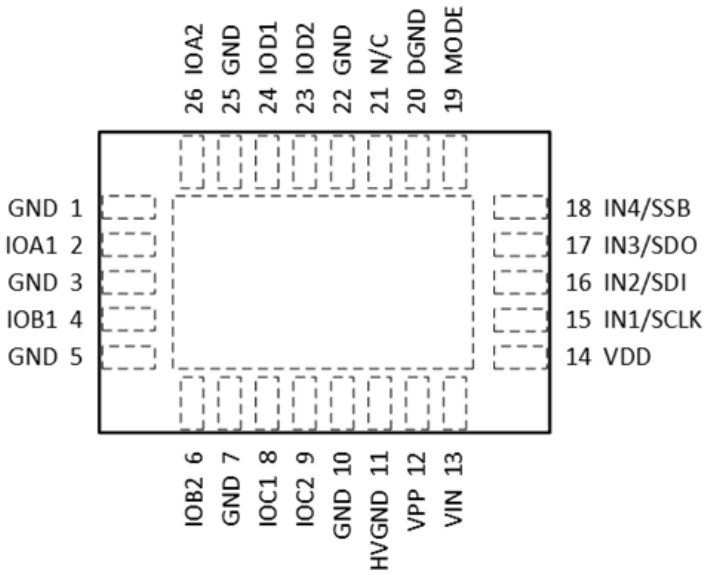
Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD	3.0	3.3	3.6	V
Supply Current	IDD		1.0		mA
Control Voltage High	V_{IH}	90% VDD			V
Control Voltage Low	V_{IL}			20% VDD	V
Operating Temperature Range	T_{OP}	-40	+25	+85	°C
Storage Temperature Range	T_{ST}	-65	+25	+150	°C

ABSOLUTE MAXIMUM RATINGS

Exceeding absolute maximum ratings may cause permanent damage

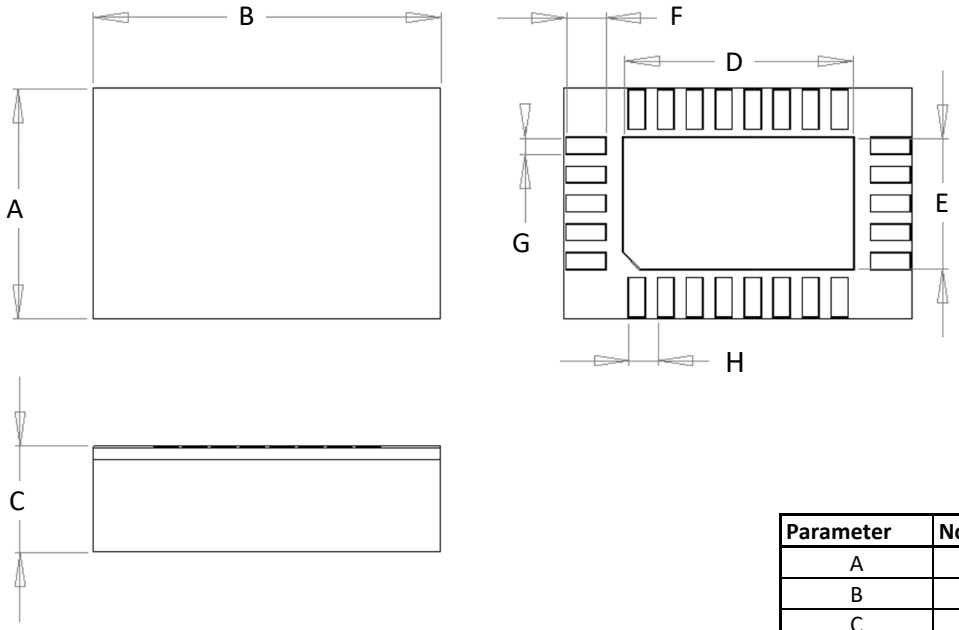
Parameter	Symbol	Conditions	Min	Max	Unit
SPST Carry Current	I_{MAX}	Any combination of DC and AC current applied to input and output	-250	250	mA
SPST Maximum voltage	V_{MAX}	Any combination of DC and AC voltage applied to input and output	-120	120	V

PIN CONFIGURATION AND FUNCTION DESCRIPTION



Number	Pin Name	Description
2	IOA1	SPST switch terminals. Switches are symmetric with input and output being fully interchangeable. When switch is turned on through SPI port the each of the number pin pairs are essentially shorted together.
26	IOA2	
4	IOB1	
6	IOB2	
8	IOC1	
9	IOC2	
24	IOD1	
23	IOD2	
1, 3, 5, 7, 10, 22, 25	GND	Ground reference pins for the low voltage driver connections. Needs to be externally shorted to Digital Ground.
20	DGND	Digital Ground
11	HVGND	Ground reference pins for the switch path devices and high voltage outputs. Needs to be externally shorted to Ground.
14	VDD	Power supply pin. Input supply for the low voltage supply. Bypass with a >1uF, 6.3V, X7R ceramic chip capacitor.
12	VPP	HV Out if Vin = 3.3 V or HV In if Vin = 0 V. Source for the High Voltage Outputs. Connect a ≥4.7nF, 100V, C0G/NPO +/-10% ceramic chip capacitor from this pin to HV Gnd.
13	VIN	3.3V supply for high voltage generator. Must be greater than VDD/2 to enable the charge pump. Bypass with a >1uF, 6.3V, X7R ceramic chip capacitor.
15	IN1/SCLK	Serial clock input when MODE = 0, GPIO input C when MODE = 1. Clock input if in SPI mode (Mode is Low) and Output A control pin if in GPIO mode (Mode is High).
16	IN2/SDI	Serial data input when MODE = 0, GPIO input D when MODE = 1. Data input if in SPI mode (Mode is Low) and Output B control pin if in GPIO mode (Mode is High).
17	IN3/SDO	Serial data output when MODE = 0, GPIO input E when MODE = 1. Data output if in SPI mode (Mode is Low) and Output C control pin if in GPIO mode (Mode is High).
18	IN4/SSB	Serial enable input when MODE = 0, GPIO input F when MODE = 1. Chip Select input if in SPI mode (Mode is Low) and Output D control pin if in GPIO mode (Mode is High).
19	MODE	Interface select, set to 0 for serial mode or 1 for GPIO mode. Dictates how the output pins are controlled. Low enabled SPI mode, so that all 4 outputs can be individually controlled. High at this pin enabled GPIO mode.

OUTLINE DIMENSIONS



Parameter	Nominal	Tolerance
A	4.00	+/- 0.10
B	6.00	+/- 0.10
C	1.80	+/- 0.10
D	4.20	+/- 0.05
E	2.30	+/- 0.05
F	0.65	+/- 0.02
G	0.35	+/- 0.02
H	0.50	+/- 0.02