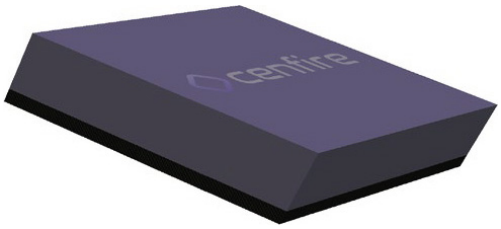
CF2140

4xSPST DC-6 GHz Switch Array



Package Diagram | 36-lead 4 x 6mm LGA package

The CF2140 4xSPST switch array is based on the Cenfire™ lowloss switching technology platform. This highly versatile product supports a wide variety of applications in signal switching and tuning with an emphasis on largescale matrix switching and high current applications. The CF2140 integrates four lowloss, fully symmetric highvoltage SPST switches with a flexible serial or parallel control interface. These switches offer industry leading capability, combining wide bandwidth with DC offset voltage support, small area, low height, and zero leakage current, making them ideal for multiplexing source and measurement units as well as routing highspeed digital signals. Additionally, the high 120 V standoff tolerance enables new applications such as Ultrasonic signal routing and RF filter tuning. The switches are normally open when off or even unpowered and will not selfactuate.

The unique, patented Cenfire™ approach represents a breakthrough in MEMS switch technology, providing superior performance, capability, and reliability over traditional solutions such as electromechanical relays, reed relays, and optocouplers.

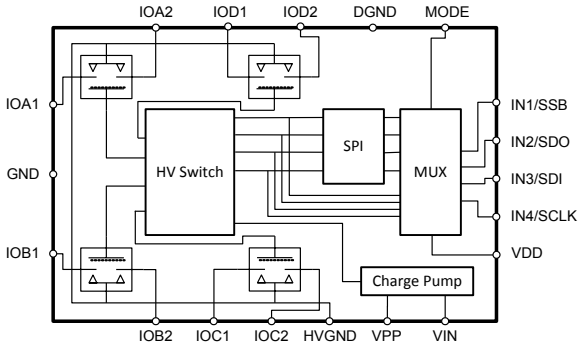
Features

- Four fully isolated SPST, NO channels
- True galvanically-isolated switching
- Digital interface with 3.3V supply
- Integrated-circuit-scale 4 x 6 mm package
- Super-fast switching time 10 µs
- True DC operation with Low 5 Ω Ron
- Low parasitic capacitance to 6 GHz
- Less than 1 nA leakage current

Applications

- Semiconductor test, relay replacement
- MRI / Ultrasound signal switching
- Battery control
- High-power RF switching, tuning, control
- GPU power control

Functional Block Diagram



Characteristics

Electromechanical Characteristics

Electrical Specifications: Unless otherwise specified, TA = TJ = 25°C, VIN = VDD = 3.3V, C_{VPP} = 4.7 nF 100V, C_{0G}/NPO +/-10%. Temperature -40°C to +85°C.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
On Resistance	R_{ON}	Resistance between SPST terminals 1 and 2.		5		Ω
On Capacitance	C_{on}	Capacitance to ground in On state, characterization		0.2		pF
Off Capacitance	C_{off}	Capacitance to ground in Off state, characterization		0.2		pF
Operating Current	$I_{operating}$	Maximum current under ordinary operating conditions		100		mA
Operating Voltage	$V_{operating}$	Maximum voltage under ordinary operating conditions			60	V
Leakage Current	$I_{leakage}$	Current from SPST terminals 1 or 2 at 50V		1		nA
Switching Time	t_{switch}	Minimum period for On to Off and Off to On state changes		10		µs
Cycling Frequency	F	Maximum cycling frequency	-	-	10	kHz
Startup Time	t_{start}	Time from VDD to all performances within specification		10		ms

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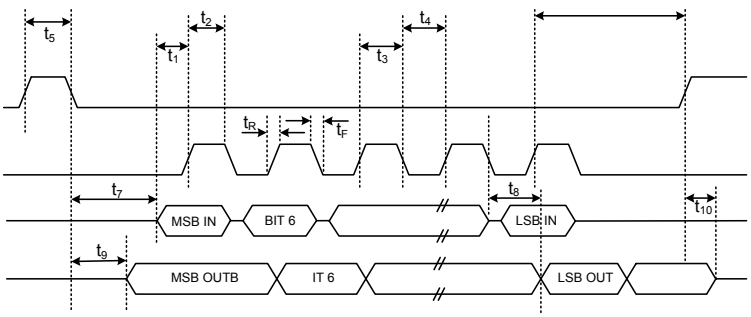


Figure 1:
SPI Timing Diagram

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Charge Pump Frequency	$f_{CP, FL}$	Full load, all switches on	–	33	–	MHz
StartUp Time	T_{ST}	No Load; time to 55V value after EN 0>1 transition	–	0.9	2	ms
Input Current through VIN	I_{IN}	Mode 0; RXB = 0x00		10		µA
Low Voltage Input Current	I_{DD}	Mode 0; RXB = 0x00		0.9		mA
Logic Input High	V_{IH}	Mode 1: Set input HI and check output	2.2	–	–	V
Logic Input Low	V_{IL}	Mode 1: Set input LO and check output	–	–	0.7	V
Logic Output High	V_{OH}	Measure at SDO pin with no load	2.97	–	–	V
Logic Output Low	V_{OL}	Measure at SDO pin with no load	–	–	0.33	V
Clock Frequency	f_{CLK}	Compare SDI and SDO data	–	5	10	MHz
Logic Input Rise/Fall Times	t_{rise}, t_{fall}	Design guidance only; 10% to 90% signal points	–	–	–	ns
SDI Valid to SCK Setup Time	t_1	Obtained by characterization , not 100% tested	10	–	–	ns
SDI Valid to SCK Hold Time	t_2	Obtained by characterization , not 100% tested	20	–	–	ns
SCK High Time (% of 1/fCLK)	t_3	Obtained by characterization , not 100% tested	45	–	55	%
SCK Low Time (% of 1/fCLK)	t_4	Obtained by characterization , not 100% tested	45	–	55	%
SSb Width	t_5	Obtained by characterization , not 100% tested	300	–	–	ns
LSb SCK to SSb High	t_6	Obtained by characterization , not 100% tested	10	–	–	ns
SSb Low to SCK High	t_7	Obtained by characterization , not 100% tested	20	–	–	ns
SDO Prop Delay from SCK fall	t_8	Obtained by characterization , not 100% tested	10	–	–	ns
SDO Output Valid after SSb low	t_9	Obtained by characterization , not 100% tested	20	–	–	ns
SSb Inactive to SDO High	t_{10}	Obtained by characterization , not 100% tested	40		–	ns

Temperature Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Temperature Range	$T_{operating}$		-40	–	85	°C

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min	Max	Unit
SPST Maximum Current	I_{Max}		-250	250	mA
SPST Maximum voltage	V_{Max}		-120	120	V
Storage Temperature Range	T_{ST}		-40	+150	°C
Low Voltage Supplies	VIN, VDD		-0.3	3.8V	V
Digital I/Os	EN, MODE, SCK, SDI, SDO, SSb		-0.3	(VDD+0.1)	V
Integrated Charge Pump	VPP		-0.3	67	V
ESD, Human Body Model, VPP pin				1000	V
ESD, Human Body Model, Other pins				200	V

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Serial Control

Serial Communication

MODE=0 activates an 8-bit SPI mode for communication. In this mode, the high voltage outputs are controlled by an 8-bit shift register used for SPI communication.

SPI Control Register

The 8bit SPI interface module consists of one 8bit Receive Register (RXB). The receive register defines the state of the 8 high voltage outputs. The data on the SDI pin is mapped such that the RXB controls the switch channel as shown in Figure 1 below. The connection map is shown in Figure 2. Note that the Most Significant bit (MSb) and the Least Significant bit (LSb) are not connected to a MEMS switch. Data is latched on the rising edge of SSb. The RXB register is cleared upon powerup.

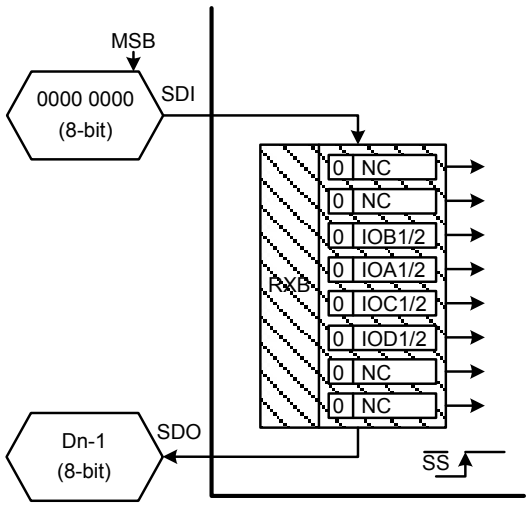


Figure 2:
RXB configuration

RXB	Channel
2	IOB1/2
3	IOA1/2
4	IOC1/2
5	IOD1/2

Figure 3:
RXB to Channel Table

SPI Interface Mode 0,00

The 8-bit SPI Interface is compatible with operation Mode 0 (CPOL=0, CPHA=0). In this mode, data is sampled at the leading rising edge of clock. The data needs to be present on the SDI pin before rising edge of the clock.

Data is pushed out of the SDO pin at the falling edge of the clock. The SDO pin can be connected to the SDI pin of another CF2140 to daisy chain multiple products.

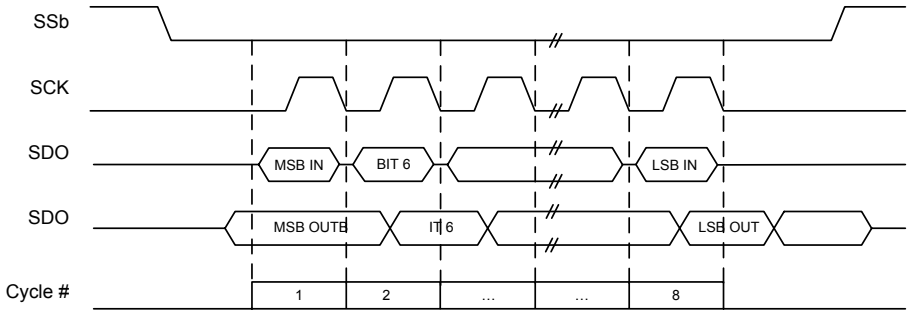
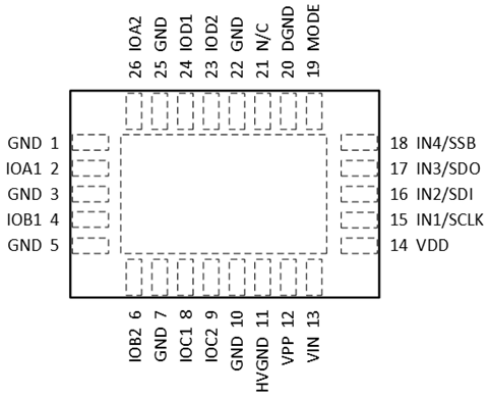


Figure 4:
SPI Mode 0 Operation

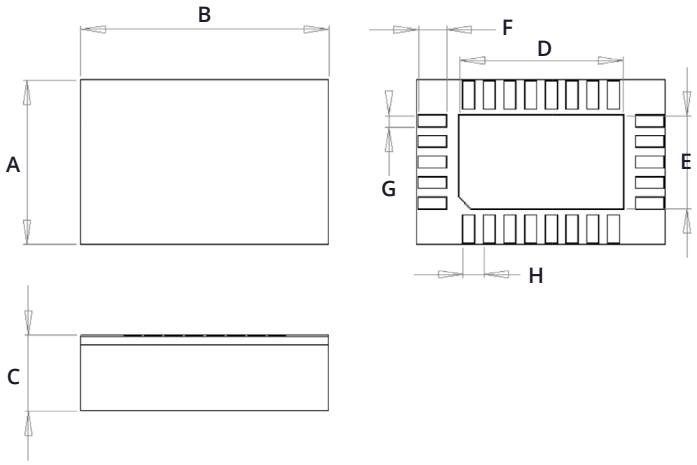
Pin Configuration and Function Description



Number	Name	Description
2	IOA1	A channel SPST switch terminals. When channel is active, pin pairs are essentially shorted together.
26	IOA2	A channel SPST switch terminals. When channel is active, pin pairs are essentially shorted together.
4	IOB1	B channel SPST switch terminals. When channel is active, pin pairs are essentially shorted together.
6	IOB2	B channel SPST switch terminals. When channel is active, pin pairs are essentially shorted together.
8	IOC1	C channel SPST switch terminals. When channel is active, pin pairs are essentially shorted together.
9	IOC2	C channel SPST switch terminals. When channel is active, pin pairs are essentially shorted together.
24	IOD1	D channel SPST switch terminals. When channel is active, pin pairs are essentially shorted together.
23	IOD2	D channel SPST switch terminals. When channel is active, pin pairs are essentially shorted together.
1, 3, 5, 7, 10, 22, 25	GND	Ground reference pins for the low voltage driver connections.
20	DGND	Digital Ground. Short to GND
11	HVGND	Ground reference pins for the switch path devices and high voltage outputs. Short to GND.
14	VDD	Power supply pin. Bypass with a >1uF, 6.3V, X7R ceramic chip capacitor.
12	VPP	Internal source for the High Voltage Outputs. Requires ≥4.7nF, 100V, C0G/NPO +/-10% ceramic chip capacitor from pin to HV Gnd. HV Out if Vin = 3.3 V or HV In if Vin = 0 V.
13	VIN	Bypass with a >1uF, 6.3V, X7R ceramic chip capacitor. Must be tied to VDD to enable the charge pump.
15	IN1/SCLK	Serial clock input when MODE = 0, GPIO closes channel B when MODE = 1.
16	IN2/SDI	Serial data input when MODE = 0, GPIO high closes channel A when MODE = 1.
17	IN3/SDO	Serial data output when MODE = 0, GPIO high closes channel C when MODE = 1.
18	IN4/SSB	Serial enable input when MODE = 0, GPIO high closes channel D when MODE = 1.
19	MODE	Interface select, set to 0 for serial mode or 1 for GPIO mode.

Outline Dimensions

Parameter	Nominal	Tolerance
A	4.00	+/- 0.10
B	6.00	+/- 0.10
C	1.80	+/- 0.10
D	4.20	+/- 0.05
E	2.30	+/- 0.05
F	0.65	+/- 0.02
G	0.35	+/- 0.02
H	0.50	+/- 0.02



Ordering Information

Order Number	Package	Packing	Minimum Order Qty	Temperature Range
CF2140-540N	LGA 26	REEL 7" Q1/T1 NDP	1500	T_{amb} = -40 °C to 85 °C

Document Categories and Disclaimer

Advance Information

The product is in the design stage with target specifications for product development. Specifications and features may change without notice.

Preliminary Specification

The datasheet contains preliminary data with additional data anticipated at a later date. Cenfire reserves the right to change specifications at any time without notice.

Product Specification

The datasheet contains final data. Cenfire will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

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